Design of Optimized Reversible Multiplier for High Speed DSP Application

Abstract—

Multipliers are the basic building blocks of a microcontroller. The speed of the multiplier determines the performance of a micro-controller. A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. Vedic mathematics is one such promising solution for increasing the speed of the multiplier. Further, implementing this in reversible logic results in power reduction. The reversible Urdhva Tiryakbhayam Vedic multiplier is one such multiplier which is effective both in terms of speed and power. In this paper we aim to enhance the performance of the multiplier by selectively decreasing the cost, garbage outputs and delay. This paper proposes an optimized design of a high speed multiplier using the techniques of vedic mathematics.

**LANGUAGE USED:**

**TOOLS REQUIRED:**

* MODELSIM – Simulation
* XILINX-ISE – Synthesis